JPL

A SYSTEMATIC APPROACH TO HARDWARE QUALIFICATION

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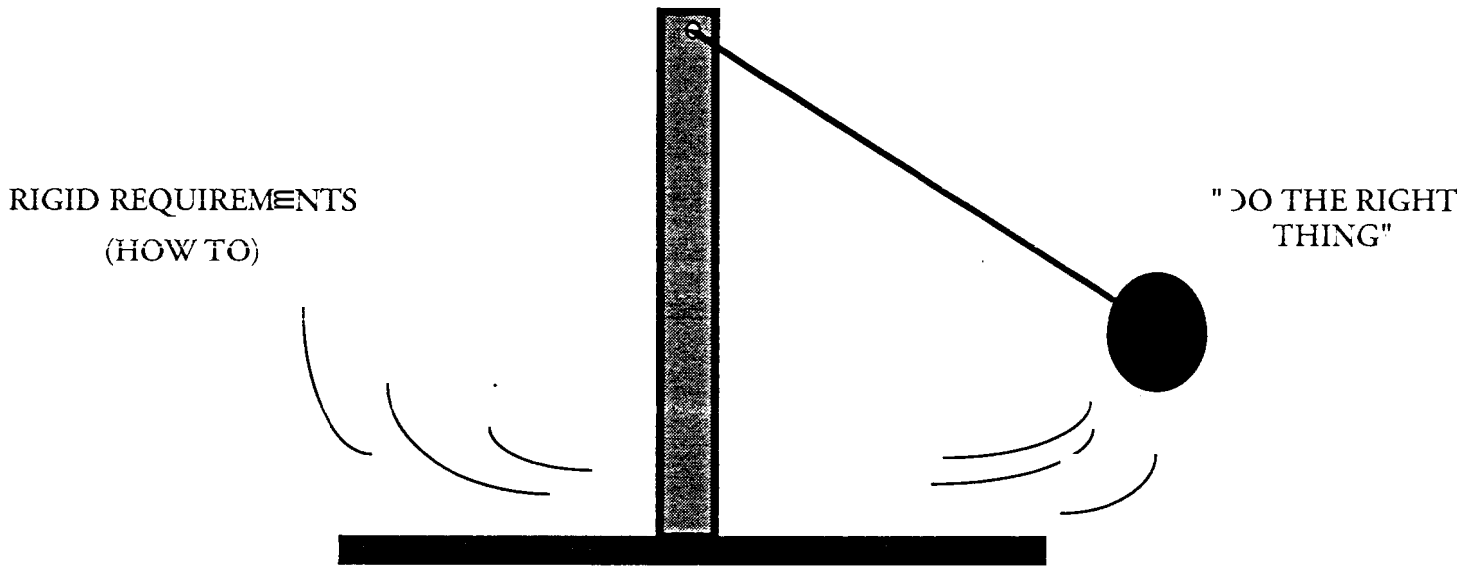
OVERVIEW

- Hardware qualification means different things to different people
  - *qualified"*
  - *"qualified by similarity"*
  - *"commercial best practices"*
  - *"performance qualified"*
  - *"it flew on Shuttle"*
- Hardware qualification should begin at the design and continue through manufacturing, integration and test
- A systematic method is required to re-engineer / streamline the qualification process
- Project management needs tools which wil allow them to make intelligent risk trade-offs in this era of greater risk taking
- Mission requirements, failure modes, technology and preventitive measures must be assessed together to determine an accurate qualification approach
- Primary thrust presented here is defect detection and avoidance

QUALIFICATION REQUIREMENTS ARE CHANGING



- Qualification requirements are changing from prescriptive to philosophical
  - *Somewhere in the middle is where we want to be*
  - *A methodology (tool) is required to assist in determining what is the "right thing"*
- An example of a technology and mission independent qualification process:
  - *NHB 5300.4 (3A-1) = : ".....shall be temperature cycled in an air oven from room temperature to -55°C to 100°C and back to room temperature at a rate not to exceed .....*
  - *NHB 5300.4 (3A-2) NOW SAYS : ".....tests shall be conducted to establish confidence in the reliability....."*

JPL DIFFICULT CHALLENGES FOR NEW MISSIONS

"USE OFF-THE-SHELF HARDWARE"

"REDUCE INSPECTION/OVERSIGHT"

"USE NEW TECHNOLOGY"

"MINIATURIZE"

"TAKE RISK BUT DON'T FAIL"

6-12 MONTH BUILD CYCLES

CHEAPER, CHEAPER & CHEAPER (BUT DON'T FAIL)

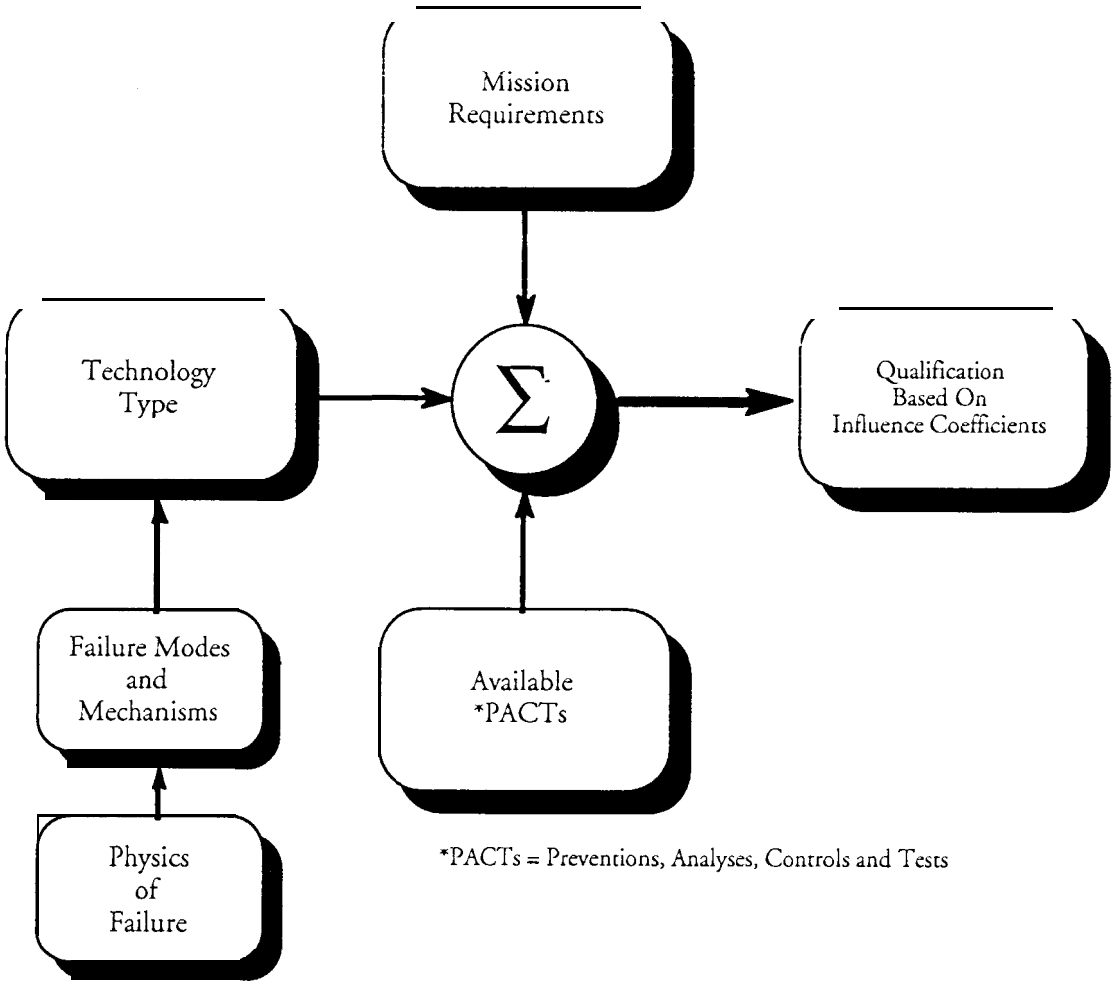
"USE INTERNATIONAL REQUIREMENTS"

PROJECT MANAGER

ELEMENTS OF HARDWARE QUALIFICATION

The aerospace industry needs to keep moving away from rigid, costly, technology independent qualification requirements

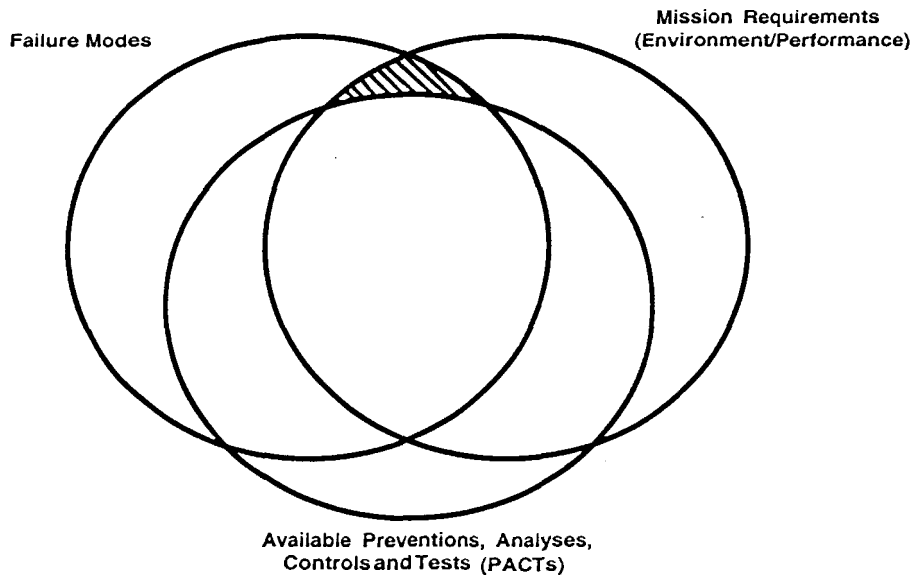
- *The RELTECH program, through ARPA and NASA Code Q is supporting this direction*



*PACTs = Preventions, Analyses, Controls and Tests

INTRODUCTION TO ACEQ

- New technologies and their associated materials and processes pose new challenges to R&QA
  - *Simply applying our existing PA techniques to the new technologies may not be adequate*
  - *New qualification methods must address real hardware failure modes and be cost effective*
- Many different approaches are used to "qualify" hardware
  - *Which ones are appropriate for our missions?*
- ACEQ (Accurate Cost Effective Qualification) was designed to identify the overlap, voids and redundancies between mission requirements, failure modes and available preventions, analyses, controls and tests (PACTs)



ACEQ IS A 4 STEP PROCESS

Step 1

Requirements
Vs.
Customer Desires

- Establish requirements
- ID Technical "Hows"
- Select Technology / Hardware

Step 2

Failure Modes
Vs.
Technology

- ID FMs for the choosen technology
  - Product Evaluations
  - Modeling
  - Vendor data/experience
  - Past peformance
  - Alerts

Step 3

Requirements
Vs.
Failure Modes

- Generate Requirements Matrix
  - ID relationships between FMs and Requirements
  - Determine the influence of the interaction

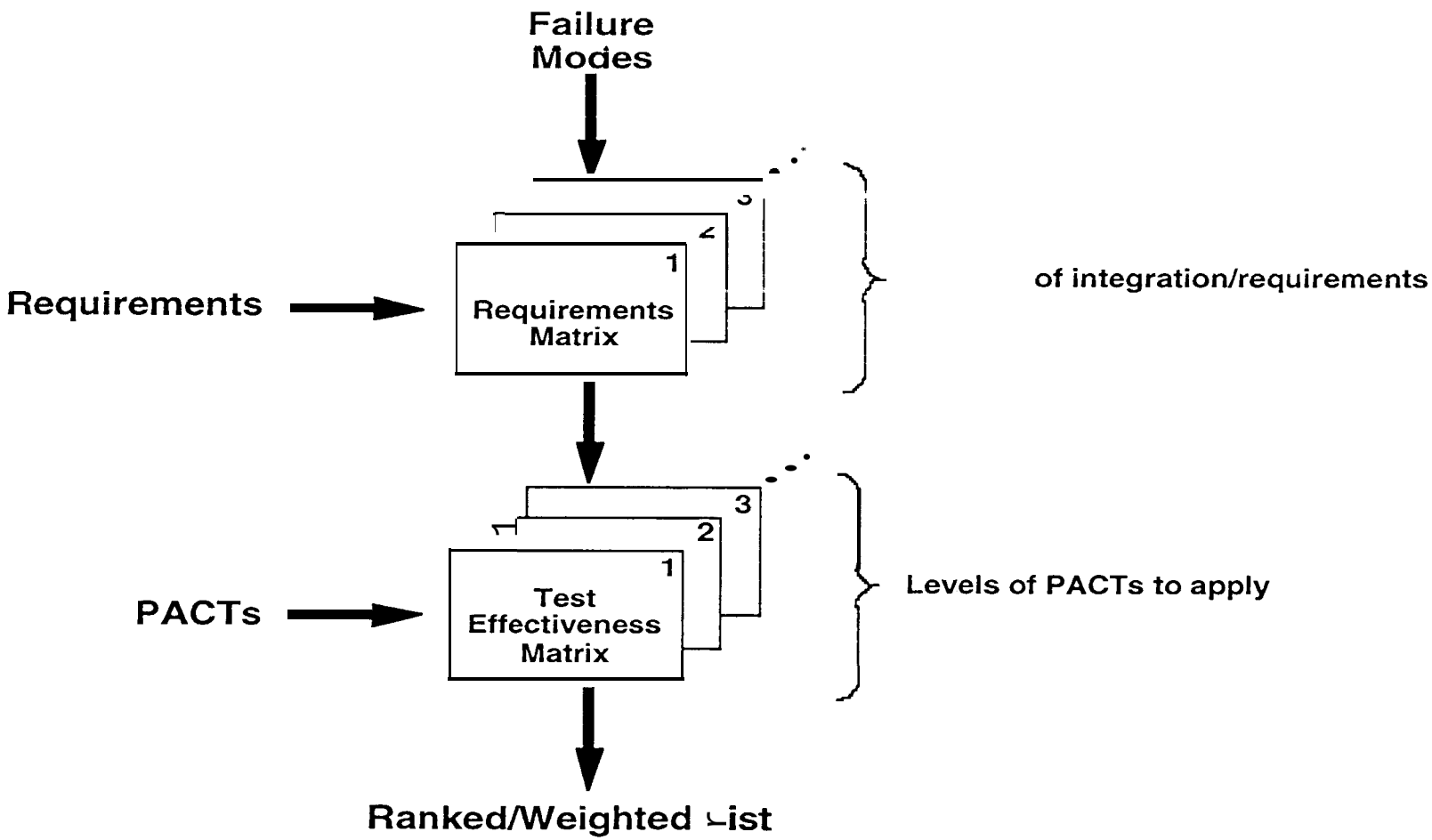
Step 4

Failure Modes
Vs.
PACTs

- Generate the Test Effectiveness Matrix
  - ID relationships between FMs and PACTs
  - Determine the influence of the interactions
  - ID overlap and redundancies in the qualification process
  - Show cost ($) of each PACT proposed
  - Rank effectiveness of PACTs
  - Recommend qualification/acceptance program

SYSTEM LEVEL APPROACH

- Each subsystem of a spacecraft/instrument will require ACEQ analysis
- Once completed, system level trades can be factored into the qualification process

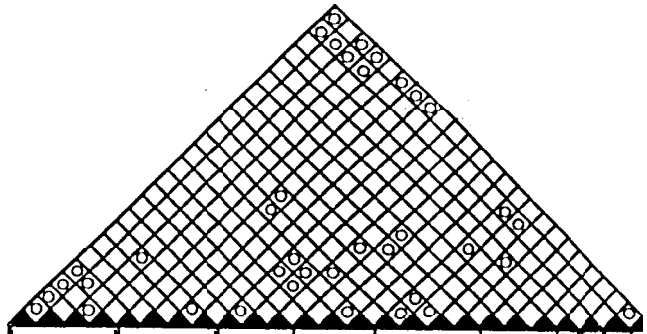


JPL STEP : ESTABLISHING THE REQUIREMENTS

CUSTOMER DESIRES ("WHATs") VS. TECHNICAL "HOWs"

FAILURE MODE IMPACT

Δ = Critical
• = Need more information at a lower level to decide

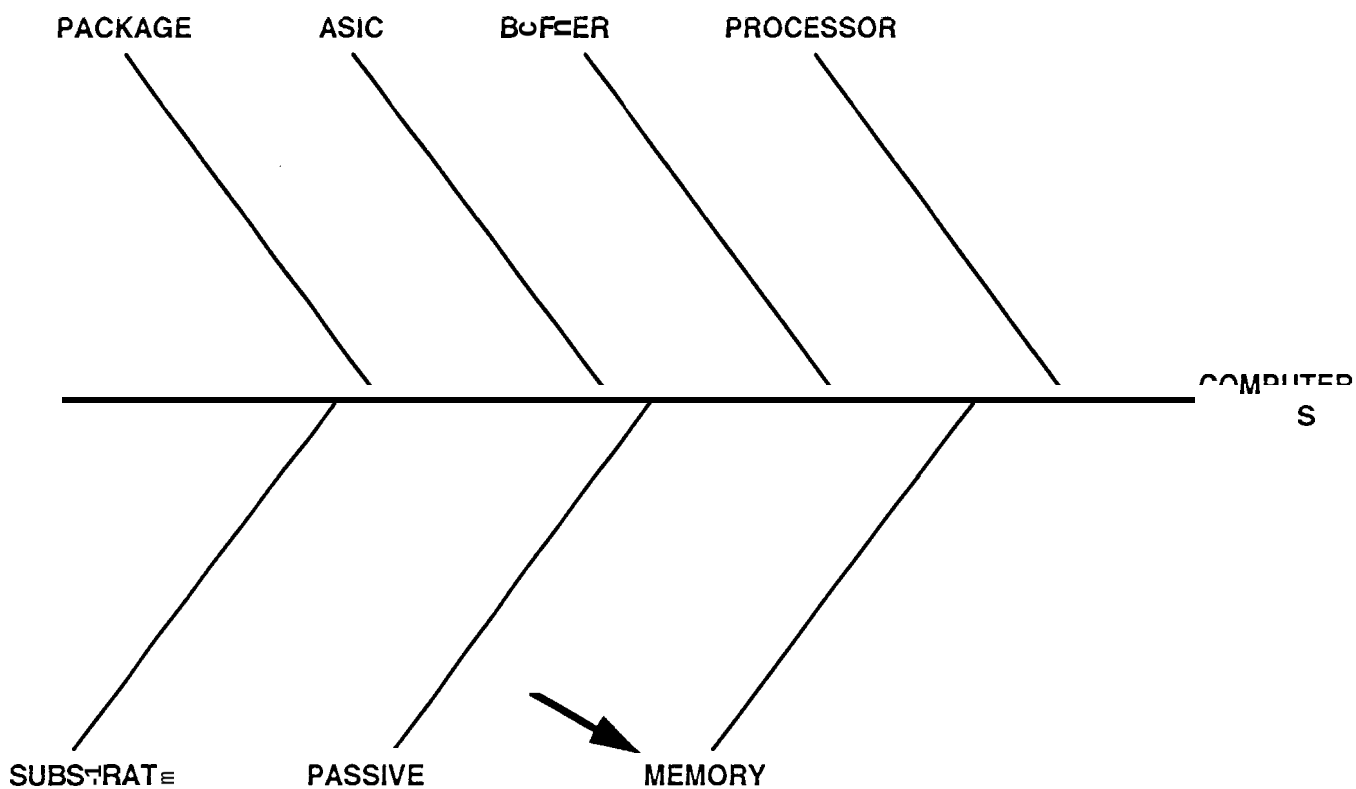


Customer Desires (mission & science) \ Ted-mid "HOWs" (subsystem level)	Telecom: 2-way comm. link (s/c and DSN)	Telecom: Uplink at S-band-comm.& telem	Telecom: Uplink at X-band - command	Telecom: Downlink at X-band - telemetry	Comm. & Data: Process. & distribut. of commands	Comm. & Data: S/C clock	Comm. & Data: Data acquisition & format	Comm. & Data: Data recording & play back	Attitu. & Artic.: Stabilization, orientation & pointing	Attitu. & Artic.: Control of propulsive maneuvers.	Attitu. & Artic.: Articulation of solar panel	Propul.: Thrust for orbit insertion	Propul.: Thrust for traj. control maneuvers	Propul.: Thrust for attitude control	Power: Energy conversion	Power: Energy storage (incl. batteries)	Power: Power control & regulation	Power: Firing of pyro squibs	Mechan.: S/C separation from TOS	Mechan.: Separation from prop. module	Mechan.: Deploy, latch - solar panel, booms	Thermal: Temp. control of S/C assemblies	Struct.: Mechanical support	Cable: Shielding, EMI protection of cables	Pyrotech.: Megalian Radar	Impact on Customer Desires	Customer Desires Criticality	Customer Desires Cost ($)
Spacecraft systems designed to have a lifetime of at least 24 months; beginning at launch (16- month cruise plus 8 months to complete one cycle of mapping).	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ			
Produce contiguous images using SAR of >70% (goal of 90%) of the surface of Venus with no periodic or systematic gaps except for one pole, with a surface radar resolution of 360 meters or better.	Δ	•	•	Δ	•	Δ	Δ	Δ	Δ	Δ	•	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	A	•	Δ	Δ	Δ			
Obtain surface brightness temperatures of greater than 70% of the Venusian surface	Δ	•	•	Δ	•	Δ	Δ	Δ	Δ	Δ	•	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	A	•	Δ	Δ	Δ			
Produce maps of the topographic and radar Scattering characteristic of the planet Venus with height resolution commensurate with the SAR range resolution and coverage commensurate with the SAR coverage. (inclination of the orbit does not permit altimetry measurements to be made within about 500 km of either pole).		•	•	Δ	•	Δ	Δ	Δ	Δ	Δ	•	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	A	•	Δ	Δ	Δ			
Refine Venus global gravity field model by combining both the MGN and Pioneer Venus Orbiter Doppler data.	Δ	•	•	Δ	•	Δ	Δ	Δ	Δ	Δ	•	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	A	•	Δ	Δ	Δ			
Technical "HOWs" impact, a																												
Cost for Technical "HOWS" ($)																												

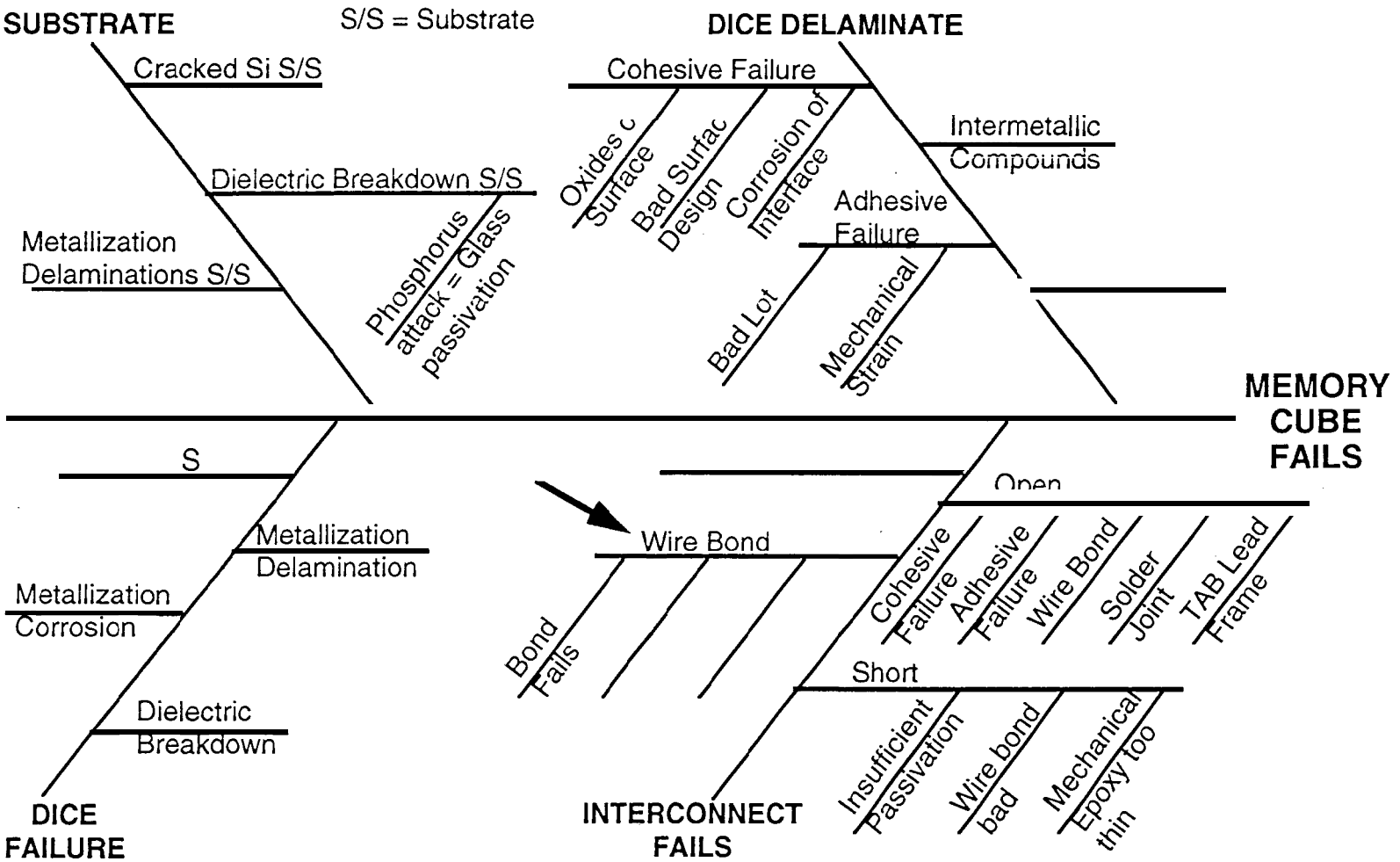
1

STEP 2 - PLOTTING THE FAILURE MODES (FMs)

- "Fish-Bone" graphs (fault trees) are used to identify failure modes and mechanisms attributed to a particular subsystem
- Information is gathered and put into a data base (sources include product evaluations, modeling, vendor experience, existing failure data, physics of failure analysis, etc.)



JPL STEP 2 - PLOTTING THE FAILURE MODES (FMs) -con't.



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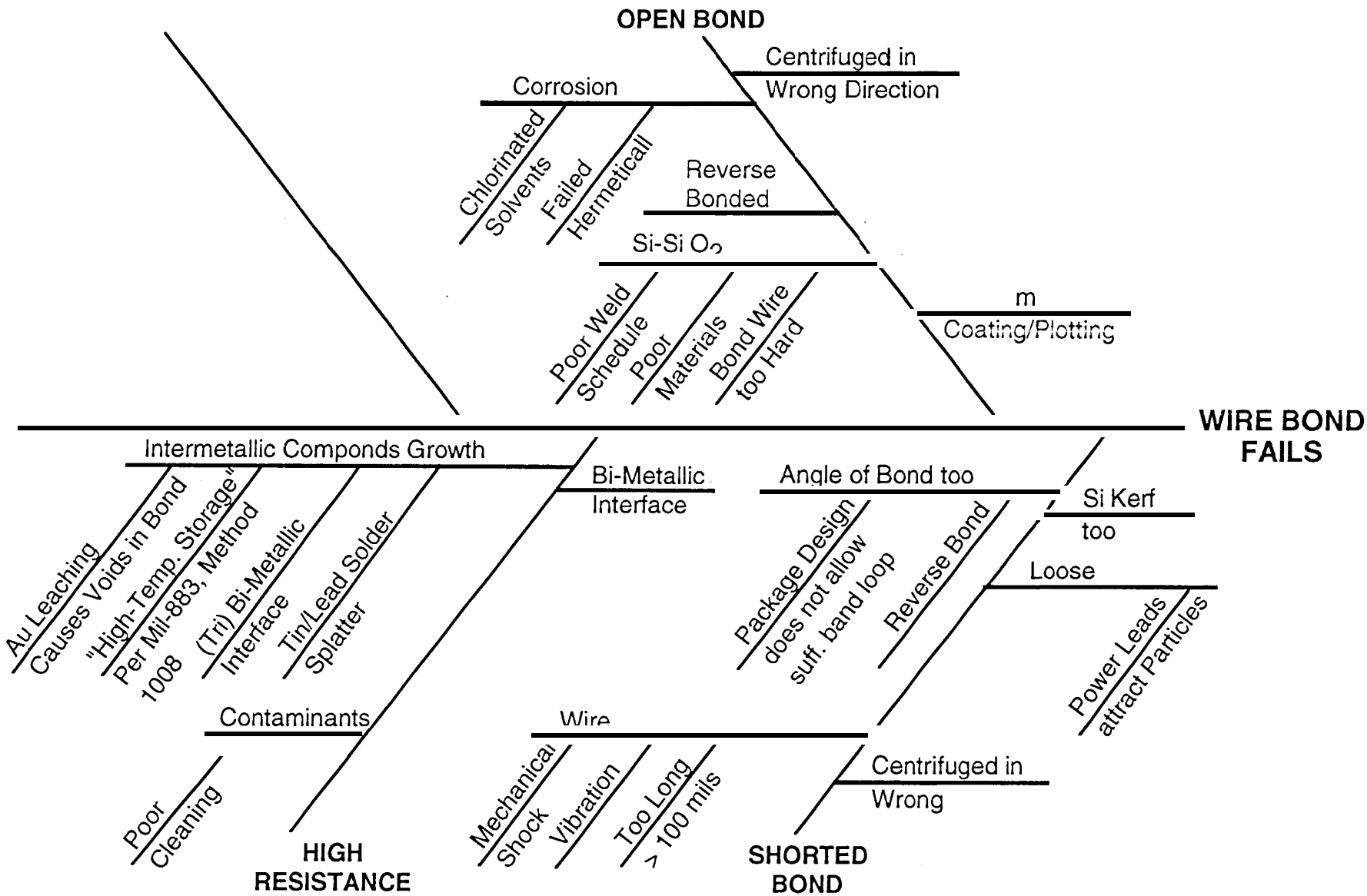

STEP 3 - PLOTTING THE REQUIREMENTS AGAINST THE FMs

REQUIREMENTS MATRIX

IMPACT LEVELS: 1 = LOW
3 = MEDIUM
9 = HIGH

WHEN (T,)	REQUIREMENTS \ FAILURE MODES	Package Fails	ASIC Fails	Buffer Fails	Processor Fails	Passives Fail	Substrate Failure	Cracked SI	Dielectric Breakdown	Metallization Delamination	Memory Cubes Fail	Dice Delamination	Cohesive Failure	Adhesive Failure	Intermetallic formation	Dice Failure	Cracked SI	Metallization Delamination	Dielectric Breakdown	Interconnect Failure	Solder Joint Failure	Wirebond Failure	Open	Shorted	Excessive Resistance	IMPACT SUMMARY (REQUIREMENTS) BEST	20	30	40	50	WORST
1	Max. Powor Diss.= 3.5W	9	1	1	3	9		9		3		9	9	9				3			9										o
2	Design Life (2+1+4 years)	9																													o
3	Memory																														
4	Eng. Data Stg.: 1 Mb	1									3																		o		
5	operating System: 10 Mb	1									3																		o		
6	Processor Board: 1 Gb	1									3																		o		
7	MaxPower Cycles																														
8	Cycles with dust storms	3				3	3			3		9	1	1		1	3	1		3	3							o			
9	Temperature Range																														
10	Ground: 5 C1040 C	1				1	3						3			1	3			3	1						o				
11	Mission: -45 C to 30 C	3	1	1	1	1							3							9	3							o			
12	Humidity: 40% to 70%	9							3																		o				
13	Vibration: E-20 Hz 1.27 cm	3				1		3					1	1	1		3				9	1	1					o			
14	20-100 Hz 10.0g							3							1								3			o					
15	Radiation: 25 krad								1																	o					
16	2000 temperature cycles	9						3						3	9	3									3			o			
17	Quasi sidy acc. 15g	3						3					1	1			3				3	1	3				o				
18	Throughput: 0.5 MIPs	1	9	3	9	1					9																				o
	Total Req. Impact	53	20	14	22	25	15	30	13	15	27	45	45	12	38	32	39	31	27	42	55	29	34	27							
	IMPACT SUMMARY (DESIGN) BEST																														
	20		o	o			o		o	o																					
	30				o	o		o			o								o			o		o							
	40														0	o	o	o		o			o								
	50											o	o	0																	
	WORST	o																			o										

STEP 4 - PLOTTING THE FMs AGAINST THE PACTs

Test Effectiveness Matrix (TEM)

SI ON SI MEMORY CUBE

	2) Die Delamination	2) Die Failures	2) Interconnection Failures	3) Solder Joint Failure	3) Wire Bond Failure	4) Open	5) Centrifuge in Wrong direction	5) Conformal Coating/Potting	5) Reverse Bonded	5) Si-SiO2 Damage	6) Poor Weld Schedule	6) Poor Materials	6) Bond Wire Too Hard	5)	6) Chlorinated Solvents	6) Failed Hermeticity	4) Shorted	5) Centrifuge in Wrong Direction	5) Silkar too large	5) Loose Particles	6) Power Leads Attract Particles	6) Vibration/Mech. Shock	5) W... Collapse	6) Mechanical Shock	6) by B...	6) Tool Longer 103+	5) Angle of bond/Design	4) High Resistance	5) Contamination/Cleaning	5) Intermetallic Compound Growth	6) Au Leaching causes voids	6) Bi Metallic Interface	6) Tin-Lead Solder Splatter	6) High Temp Storage (per M S-883)	TEST EFFECTIVENESS COEF	PREVENTION/ANALYSIS/CONTROL/TEST COST (K$)	EFFECTIVE LEVEL TO PERFORM	VENDOR PERFORMS?
[redacted]		1																																				
[redacted]																																						
[redacted]																																			1	1		
[redacted]																													3						3	3		Y(1)
LEAD FINISH INSPECTION					3																										1	1			5	1		
SOLD. FILLET THICK. = 2-7 MILS					3																														3	1		
100% DIE CRACK/DEFECT INSP.																			1																1	3		Y(3)
PARAM. DIE LEVEL TESTING																																			0	2		
OPTICAL INSPECTION								1		3	3				1			1	3								3			1			3		19	4		Y(5)
CONFORMAL COATING INSP.																																						
MATERIAL VISCOSITY																																						
PULL/SHEAR TEST/FLEX TEST					3								3	3																					9	3		
CHECK FOR AIR BUBBLES																																			0	1		
DIELECTRIC MATL CONTROLS																													1						1	0		Y(1)
WELD SCHEDULE												9		3													9								21	1		
PIND TESTING																				9						3							9		21	5		
GOLD WIRE PURITY CHECK																				3									3	1					7	1		
HERMITICITY CHECKS																																			0	0		Y(3)
INITIAL HANDLING CONTROL																													1						1	1		
NAMICS																																						
RANDOM/SINE																																						
[redacted]																																						
SHOCK					3																														3	4		
[redacted]																																						Y(8)
[redacted]																																						
[redacted]																																						
WORST CASE ANALYSIS																					3							3							6	8		
[redacted]																																						
CONSTRUCTION																																						
MATERIALS																																						
MECHANICAL					1						3																		1						5	5		
DEGRADATION					1									3																	3				7	8		
[redacted]																																						
STRAIN/EL																																						
DIELECTRIC MEASUREMENTS										1																									1	0		Y(1)
ELEC. PERF. TESTING				3	9		9		3												3							3							21	6		
DESIGN																																						
CIRCUIT REDUNDANCY																																			0	3		
STAGGERED VIAS																																			0	2		
THERMAL MANAGEMENT													1																	3					4	5		
MATERIALS SELECTION					1				1		1		9		3	9													1	1	3				29	5		
ACCESSIBILITY OF FAILURE MODE TO PREVENTION/ANALYSIS/CONTROL/TEST				3	42		9	1	10	3	9	9	14	6	16	11	0	6	1	4	18	7	18	3	10	10	3	12	7	18	16	9	8	12	9	$118	TOTAL k$	
																																				$72	Tot. eff > 5	
																																				$38	Tot. eff > 10	

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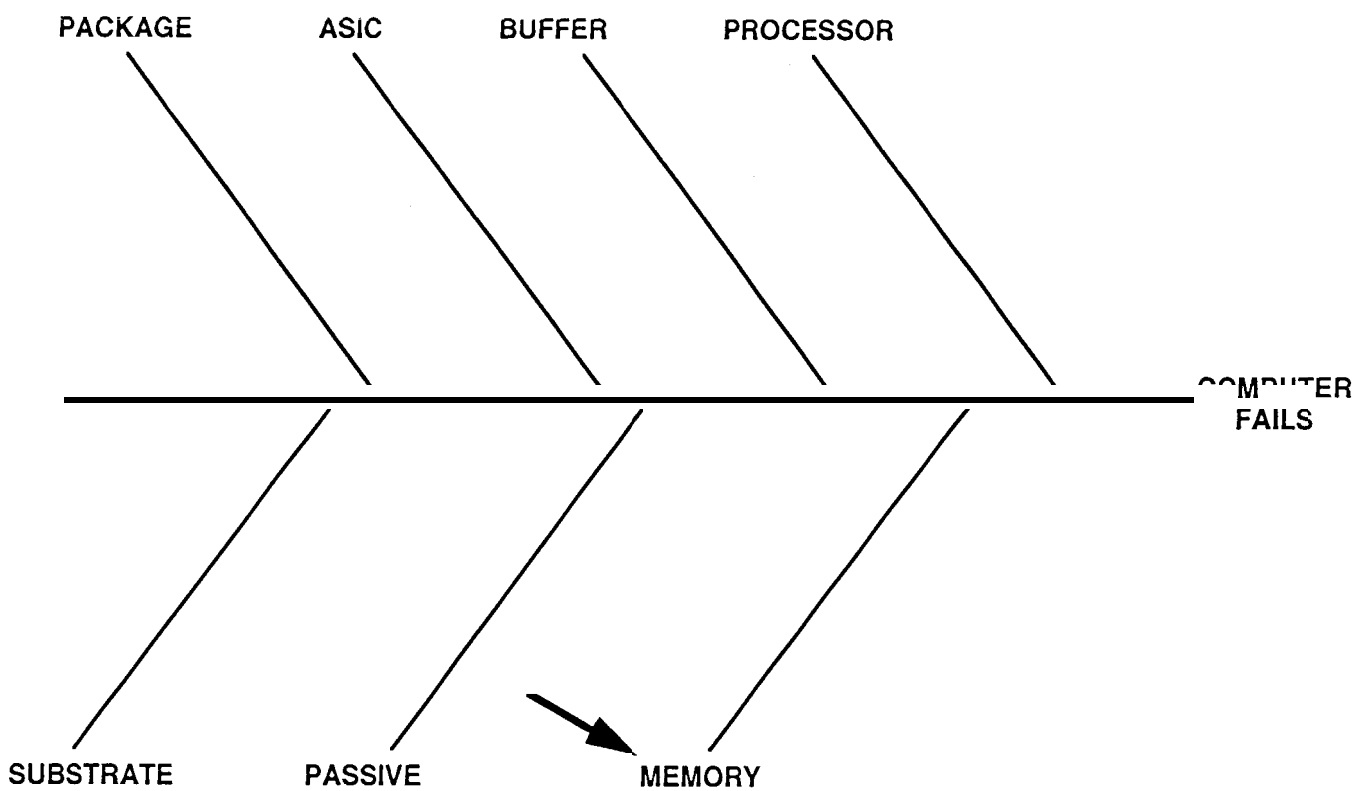

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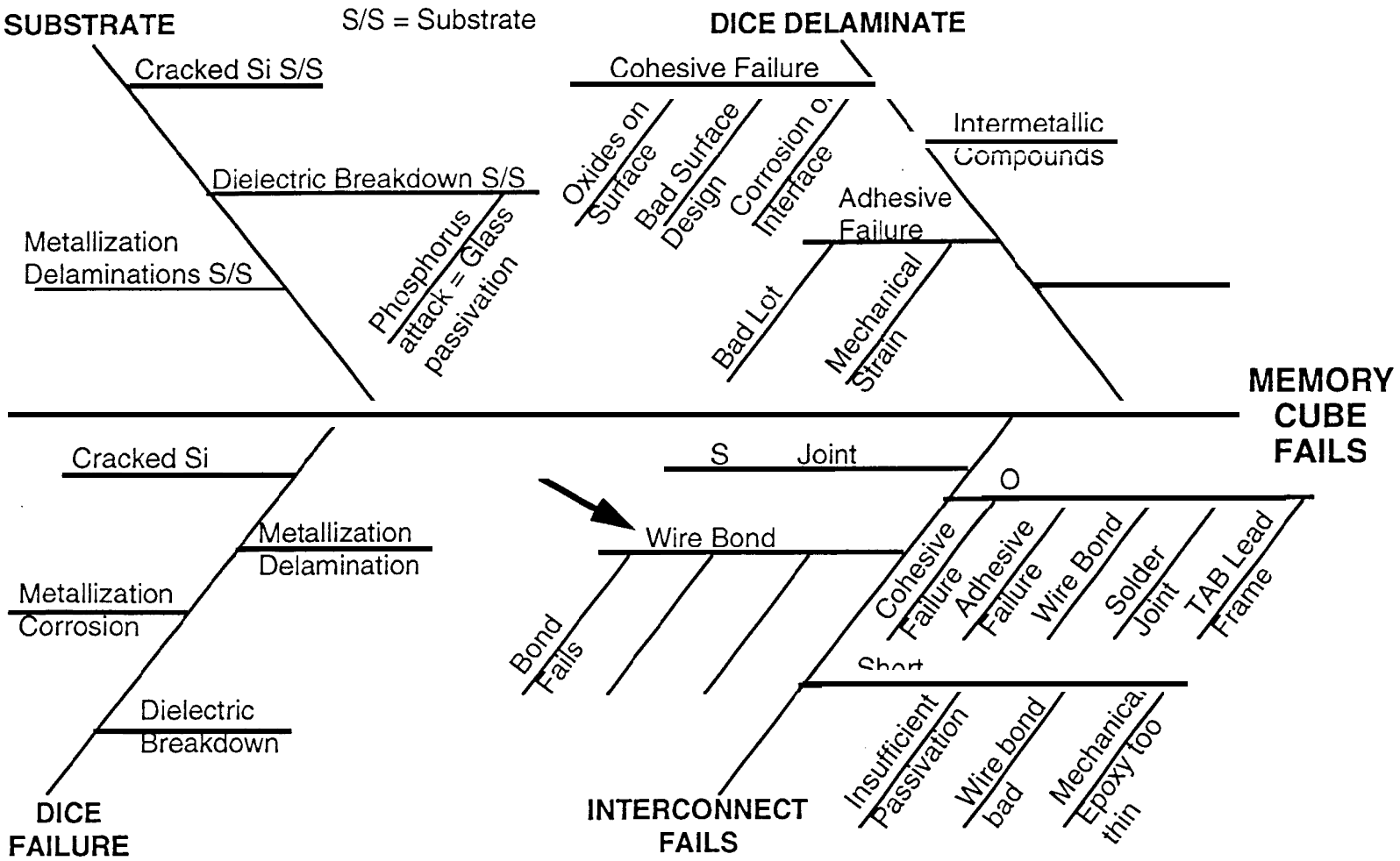
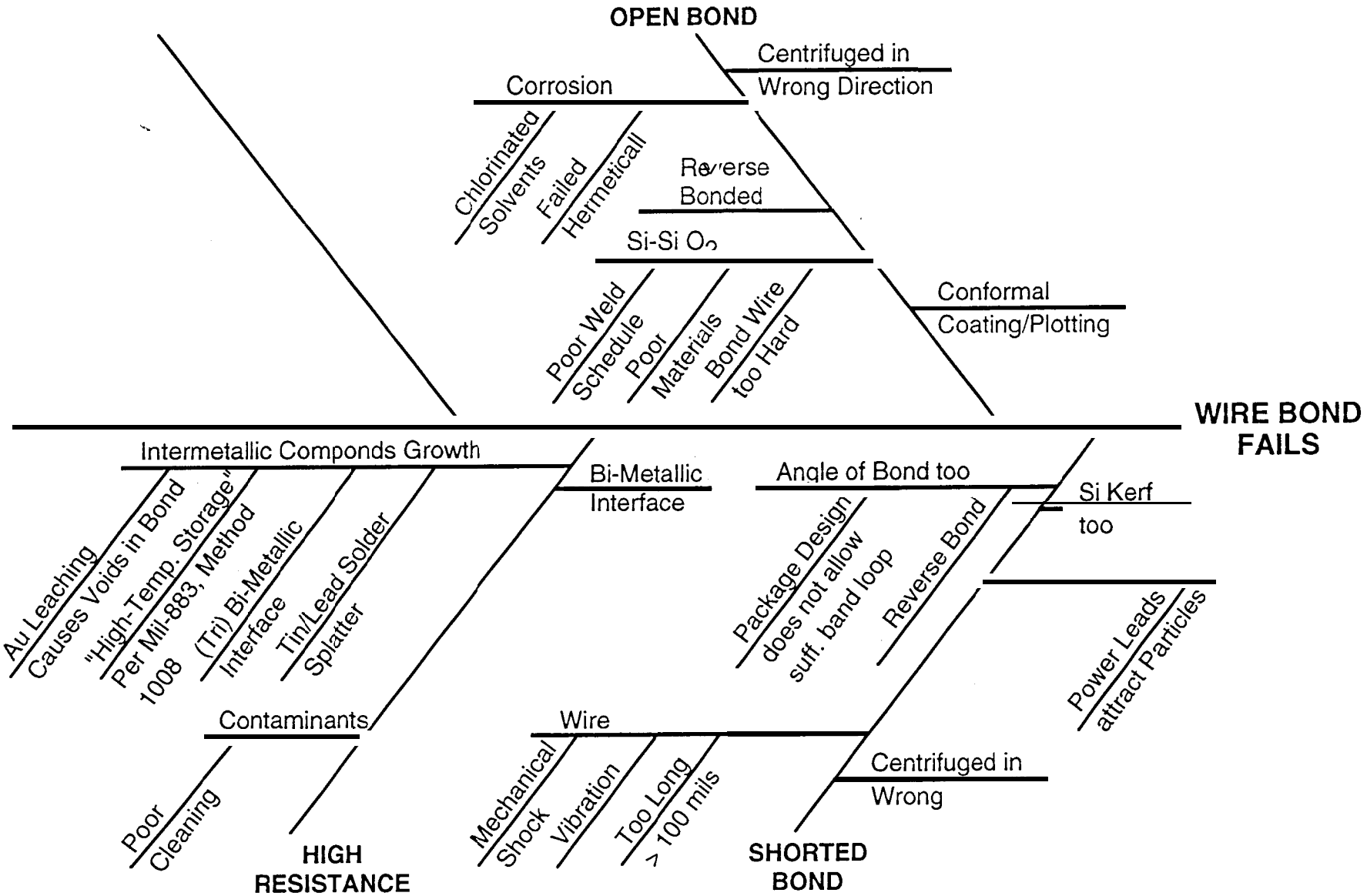


S.L. Cornford

JPL S' 'EP 2 - P_OT' ' NG ' 'HE FA .URE MODES (FMs -con't.



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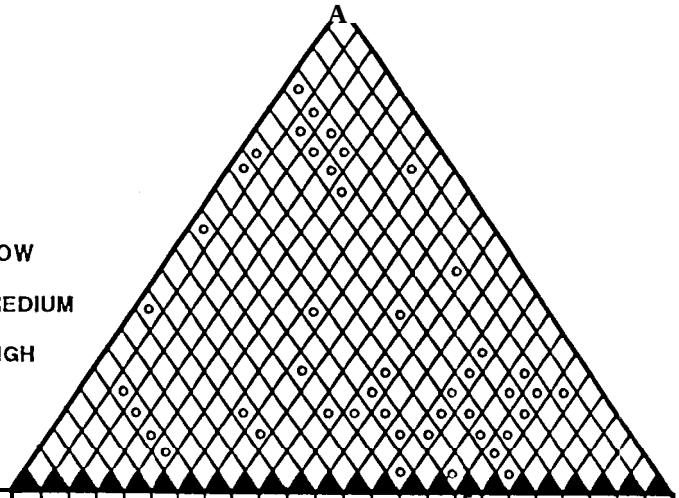

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1		Max. Prover Diss. =3.5W	9	1	1	3	9		9		3		9	9	9				3			9										o
2		Design Life (2+1 +4 years)	9	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→						o
3		Memory																														
4		Eng. Data Stg.: 1 Mb	1									3	→	→	→	→	→	→	→	→	→	→	→	→	→	→					o	
5		Operating System: 10 Mb	1									3	→	→	→	→	→	→	→	→	→	→	→	→	→	→					o	
6		Processor Board: 1 Gb	1									3	→	→	→	→	→	→	→	→	→	→	→	→	→	→					o	
7		Max Power Cycles																														
8		Cycles with dust storms	3				3	3			3		9	1	1		1	3	1		3	3								o		
9		Temperature Range																														
10		Ground: 5 C1040 C	1				1	3						3			1	3			3	1						o				
11		Mission: -45C1030 C	3	1	1	1	1							3							9	3							o			
12		Humidity: 40% to 70%	9							3																		o				
13		Vibration: 5-20 Hz 1.27 cm	3				1		3					1	1	1		3				9	1	1					o			
14		20-100 Hz 10.0g							3							1								3			o					
15		Radiation: 25 krad								1																	o					
16		2030 temperature cycles	9						3						3	9	3									3			o			
17		Quasi stdv ace. 15a	3						3					1	1			3				3	1	3				o				
18		Throughput: 0.5 MIPs	1	9	3	9	1					9	→	→	→	→	→	→	→	→	→	→	→	→	→	→						o
		Total Req. Impact	63	20	14	22	25	15	30	13	15	27	45	45	42	38	32	39	31	27	42	55	29	34	27	30						
		IMPACT SUMMARY (DESIGN) BEST																														
		20		o	o			o		o	o																					
		30				o	o		o			o								o			o		o	o						
		40														o	o	o	o		o			o								
		50											o	o	o																	
		WORST	o																			o										
		WHEN (T,)																														

STEP 4 - PLOTTING THE FMs AGAINST THE PACTs

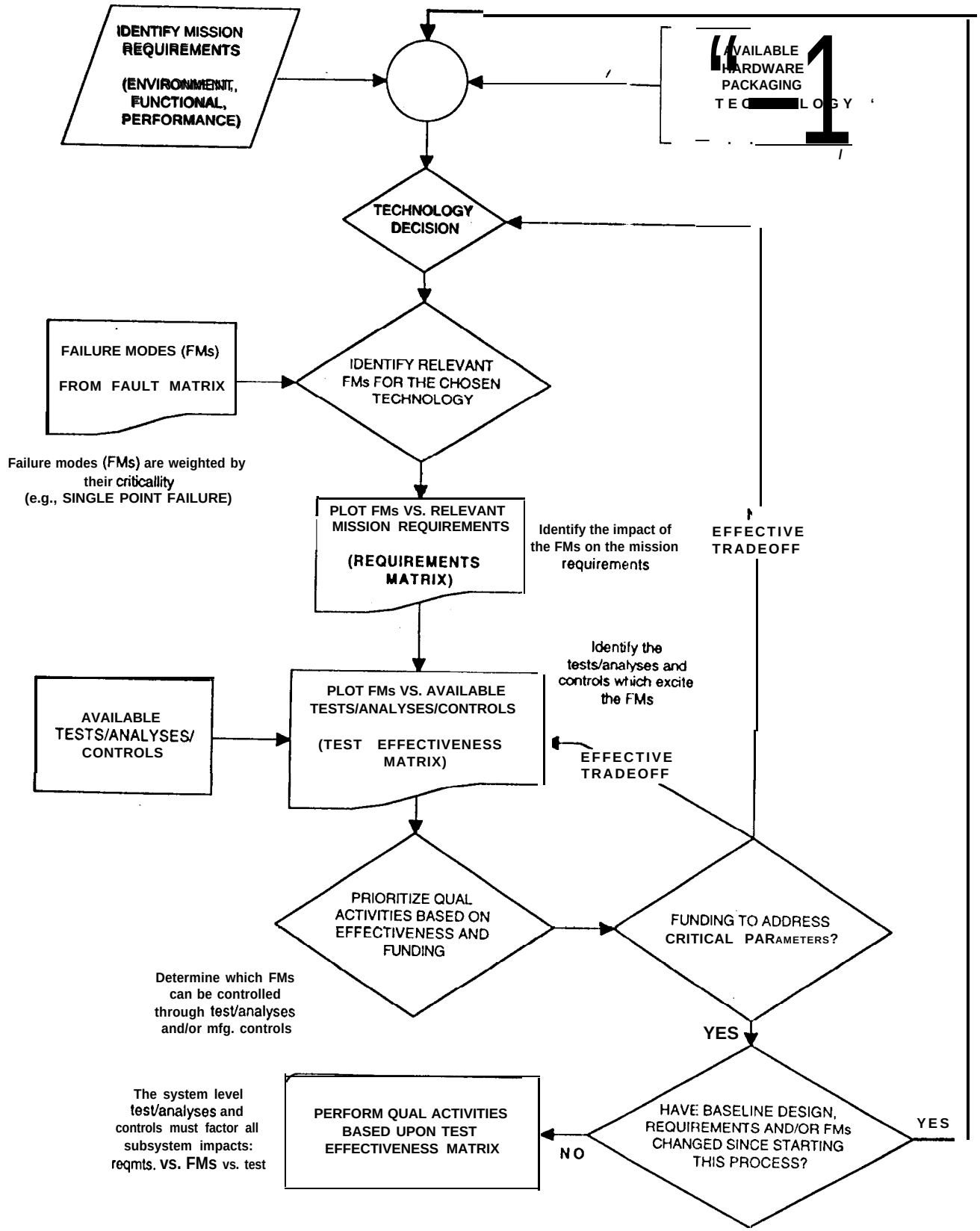
Test Effectiveness Matrix (TEM)

SI ON SI MEMORY CUBE

	Dice Delaminations	Dice Failures	Interconnection Failures	Solder Joint Failure	Wire Bond Failure	Open	Centrifuge in wrong direction	Conformal Coating/Potting	Reverse Biased	Bi-SiO2 Damage	Poor Weld Schedule	Poor Materials	Bond Wire Too Hard	Corrosion	Chlorinated Solvents	Failed Hermiticity	Shorted	Centrifuge in Wrong Direction	Si Kerf too large	Loose Particles	Power Leads Attract Particles	Vibration/Mech. Shock	Wire Collapse	Mechanical Shock	Vibration	Too Long >100mil	Angle of bond/Design	High Resistance	Contamination/Cleaning	Intermetallic Compound Growth	Au Leaching causes voids	Bi-Metallic Interface	Tin-Lead Solder Splatter	High Temp Storage (per M-S-883)	TEST EFFECTIVENESS COEFFICIENT	PREVENTION/ANALYSIS/CONTROL/TEST COST (K$)	EFFECTIVE LEVEL TO PERFORM	VENDOR PCN? OK w/S?
	2)	2)	2)	3)	3)	4)	5)	5)	5)	5)	6)	6)	6)	5)	6)	6)	4)	5)	5)	5)	6)	6)	5)	6)	6)	6)	5)	4)	5)	5)	6)	6)	6)	6)				
REQ. INFLUENCE COEFF.	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
MFG / QA CONTROLS																																						
MATL OUTGAS, REQMT. & TEST																													1						1	1		
OPTIC. CLEANL. PROD/INSP.																													3						3	0		Y(1)
LEAD FINISH INSPECTION					3																										1	1			5	1		
SOLD. FILLET THICK. = 2-7 MILS					3																														3	1		
100% DIE CRACK/DEFECT INSP.																				1															1	3		Y(3)
PARAM. DIE LEVEL TESTING																																			0	2		
OPTICAL INSPECTION							1			3	3				1				1	3							3				1			3	19	4		Y(5)
CONFORMAL COATING INSP.																																			0	2		
MATERIAL VISCOSITY									3				1																						4	1		
PULL/SHEAR TEST/FLEX TEST					3									3	3																				9	3		
CHECK FOR AIR BUBBLES																																			0	1		
DIELECTRIC MATL CONTROLS																													1						1	0		Y(1)
WELD SCHEDULE											9			3													9								21	1		
PIND TESTING																					9					3								9	21	5		
GOLD WIRE PURITY CHECK																					3								3	1					7	1		
HERMITICITY CHECKS																																			0	0		Y(3)
INITIAL HANDLING CONTROL																													1						1	1		
DYNAMICS TESTING																																						
RANDOM/SINE					3												3			3		9		1	9										28	9		
SHOCK					3												3			3		9		9	1										26	9		Y(7)
THERMAL TESTING																																						
DWELL					1										3														3	9	1	3		9	29	9		
SHOCK					3																														3	4		
CYCLE					9																										1		3		13	0		Y(10)
RADIATION																																						
DOSE RATE 1																																			0	10		
HUMIDITY															3	1													3			1			8	6		
WORST CASE ANALYSIS																						3						3							6	8		
FMECA					1																	1						1							3	4		
CONSTRUCTION ANALYSIS																																						
MATERIALS					1				3		1		3			1													1		1				11	5		
MECHANICAL					1						3																		1						5	5		
DEGRADATION					1										3																	3			7	6		
TESTS/ANALYSES																																						
FIBER STRAIN/ELONG. TEST																								3											3	2		
DIELECTRIC MEASUREMENTS											1																								1	0		Y(1)
ELEC. PERF. TESTING				3	9		9		3													3						3							21	6		
DESIGN																																						
CIRCUIT REDUNDANCY																																			0	3		
STAGGERED VIAS																																			0	2		
THERMAL MANAGEMENT													1																	3					4	5		
MATERIALS SELECTION					1				1		1		9		3	9													1	1	3				29	5		
ACCESSIBILITY OF FAILURE MODE TO PREVENTION/ANALYSIS/CONTROL/TEST				3	42		9	1	10	3	9	9	14	6	16	11	0	6	1	4	18	7	18	3	10	10	3	12	7	18	16	9	8	12	9	$118	TOTAL k$	
																																				$72	Tot, eff > 5	
																																				$38	Tot, eff > 10	

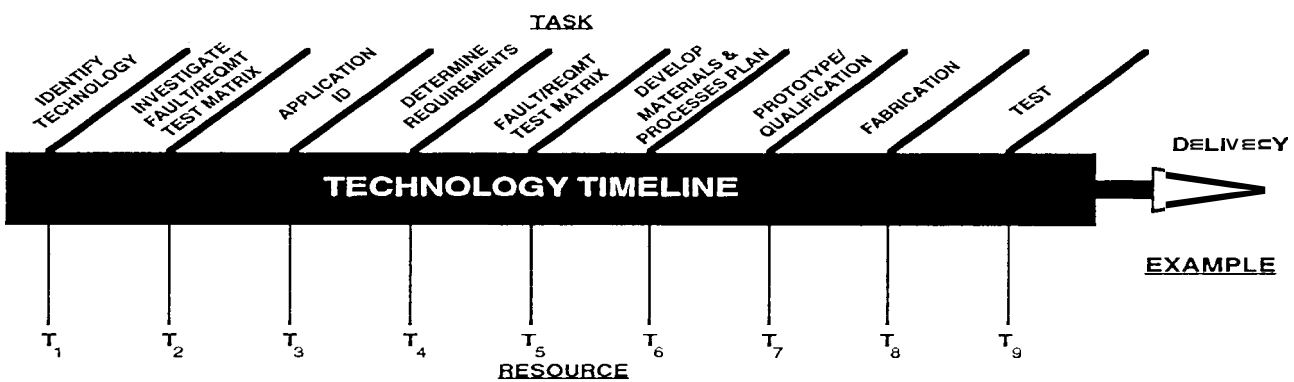
S. Cornford

PHYSICS OF FAILURE BASED HARDWARE QUALIFICATION



JPL

ACEQ FLOW CHART

CONCLUSION TO ACEQ

- This process will allow a systems approach to permit trade-offs and risk assessment by the project
- Provides continuity between projects on how qualification and acceptance processes are established
- Allows vendor performed activities to factor into the qualification process - off-the-shelf hardware
  - *Hardware buyer/integrator can determine if the failure modes for a particular mission have been addressed*
- Once the effects of Requirements vs. Failure Modes vs. PACTs are identified:
  - *Careful prioritization and trade-offs must take place*
  - *The process and decisions are documented*
- This process will help the project understand resource allocation required to address the qualification process throughout product development / procurement